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A Novel Multilevel Inverter with Reduced DC Sources

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Abstract: Multilevel inverters have become more popular in high power and high voltage application. They have a unique structure which makes it possible to reach high voltages with less harmonic content. Harmonic content of the output voltage waveform decreases as the number of output voltage level increases. The main advantages are lower Total Harmonic Distortion (THD), less stress on the power switches and higher efficiency. However, increase in the device count due to increased voltage levels makes the control method complex and hence expensive. This paper presents a nine level inverter with reduced DC sources which is capable of obtaining all additive and subtractive combinations of input DC levels. This topology requires less power switches compared to conventional multilevel inverter and less gate drives. The proposed topology is presented through a nine-level inverter with an appropriate modulation scheme and detailed simulation has been carried out in MATLAB/Simulink. A comparison is made between proposed topology and the conventional multilevel topology on the basis of device count, number of levels in the output voltage and THD.

Keywords: Multilevel Inverter (MLI); Phase Opposition Disposition SPWM; Power Electronics; Total Harmonic Distortion (THD).

I. INTRODUCTION

In the last few decades, multilevel voltage-source inverters have emerged as a viable solution for high-power dc-to-ac conversion applications [1]. A multilevel inverter (MLI) is a linkage structure of multiple input dc levels (obtained from dc sources and/or capacitors) and power semiconductor devices to synthesize a staircase waveform. Voltage stresses experienced by the power switches are lower as compared to the overall operating voltage level [2]. In addition, the multilevel waveform has a better harmonic profile as compared to a two-level waveform obtained from conventional inverters. Other advantages of MLIs are reduced *dv/dt* stress on the load and possibility of fault-tolerant operation [3]. Researchers are also exploring avenues to employ MLIs for low-power applications [4]. The multilevel inverters are used in drives, PV systems and automotive applications.

The quality of the multilevel waveform is enhanced by increasing the number of levels. However, it inadvertently leads to a large number of power semiconductor devices and accompanying gate driver circuits. This increases system complexity and cost and tends to reduce the system reliability and efficiency. For a high-resolution waveform, therefore, practical considerations necessitate reduction in the number of switches and gate driver circuits [5]. The topologies which have been extensively studied and are commercially available for multilevel voltage output are neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) converters [1], [3], [5]–[7]. However, there is a significant increase in the number of power switches, the number of switches conducting simultaneously, and the overall cost of the system with the increase in the number of output levels. Researchers, therefore, continue to focus on reducing the component count in multilevel topologies through various approaches. The main disadvantage is the increase in number of power switches that normally contributes to the complexity in controlling the power switches. Many methods have been developed to decrease the number of switches [8]. Modulation strategies applied to multilevel inverters are selective harmonics elimination [9] [10], carrier based pulse width modulation [11] [12], space vector modulation [13] [14] and fundamental frequency modulation [15] [16]. The pulse-width modulation (PWM) control [17] is the most efficient method of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. In this paper, a new topology is proposed in which the use of dc sources are reduced via power switches. This approach significantly lessens the number of power switches needed as compared to the conventional topologies.

This paper proposes a nine-level inverter with reduced DC sources which requires less number of switches than conventional topologies. Section II presents the conventional nine-level inverter. Section III describes the proposed nine-level inverter. The working principle along with DC source arrangement, working states and modulation scheme are discussed in section IV. In section V, simulation results are detailed. Conclusions are summarized in section VI.

II. CONVENTIONAL NINE-LEVEL INVERTER

The generalized single-phase structure of the conventional [18] topology is shown in Fig. 1. It has n number of isolated input dc sources. The linkage structure is such that

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the higher potential terminal of the preceding source is connected to the lower potential terminal of the succeeding source and vice versa through power switches. Input sources are designated as E_j (where j = 1 to n). Source current from each source is designated as i_j(t). Power switches can be implemented using a transistor device [e.g., MOSFET and insulated-gate bipolar transistor (IGBT)] with an antiparallel diode. In Fig. 1, power switches are illustrated with IGBTs with antiparallel diodes, and complementary pairs are designated as (T_j, T'_j) (where j = 1 to n + *1*). Various nodal voltages are indicated as vj(t) (where j = 1 to n + *1*). Load voltage and load current are designated as v_L(t) and i_L(t), respectively. In case of a nine-level inverter it requires ten number of switches connected in the same pattern as given in the generalized structure with four dc sources. According to this topology, as the number of level increases the number of switches and the use of sources also increases which adds up to the cost and makes the circuit more complex. When a fault occurs it is possible to replace it quickly. In nine level inverter it will be having five pairs of active switches (T_j, T'_j) (j = 1, 2, 3, 4, 5) with E_1, E_2, E_3 and E_4 as the input DC sources. By operating the inverter with suitable modes, it supplies the load with nine levels, viz., $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$ and zero for $E_1 = E_2 = E_3 = E_4 = V_{dc}$ (symmetric source configuration). The maximum number of levels synthesized by this topology is 2n+1, where n is the number of sources. It requires less number of components comparative to the diode clamped or the flying capacitor or cascaded configuration. For 'n' levels it requires n number of sources and n+1 number of power switches.

From Fig.1, it is clearly understood that the circuit become more complex for higher number of levels as it increases the use of sources and switches. It is also important to mention here that dc source voltages have been assumed to be equal in this work. In practice, they might differ (e.g., due to different states of charge of batteries or due to shading of some cells if the sources are coming from a photovoltaic (PV) system). To account for this variation and to reduce the number of switches and sources for higher levels, a new topology is developed which is described in section III.

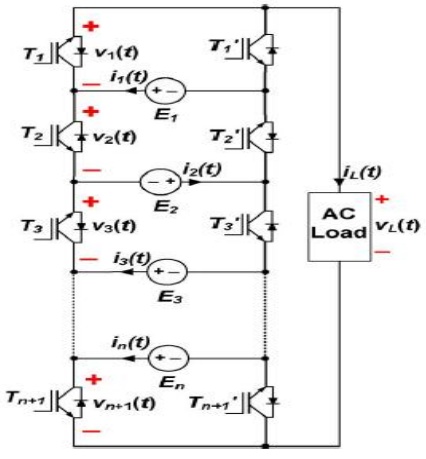

Fig.1 Generalized single-phase structure of conventional topology

III. PROPOSED NINE-LEVEL INVERTER

Conventional cascaded multilevel inverters require large number of switches. In the proposed multilevel inverter there is no need to use all the switches; the structure should be such that it can synthesize all the additive and subtractive combinations of the input DC levels. Moreover, depending on the selection of the voltage levels of sources, each 'step' in the output waveform so obtained is uniformly equal to the smallest input DC level. The generalized multilevel inverter topology based on the aforesaid concept is also presented.

The concept adapted for the proposed MLI topology is that the inverter should be capable of synthesizing all possible additive and subtractive combinations of the DC levels of the input sources. Some examples of such combinations are as follows:

(a) With single DC source:

If a single DC source of voltage $E1$ is present, the possible combinations are: $+E1$, 0 and $-E1$. The resultant inverter can be a three-level or two-level (when zero level is excluded) inverter. Such a structure is shown in Fig. 2a. It is a standard single-phase full bridge inverter.

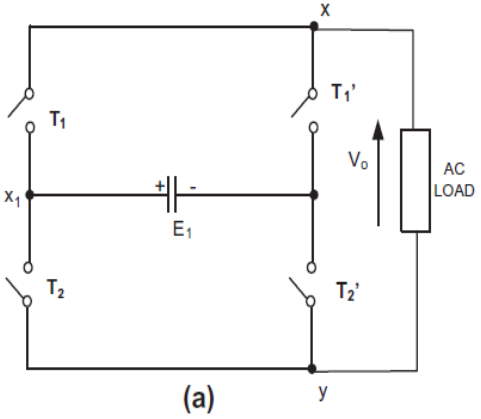

Fig.2a Inverter structure with single DC source

(b) With two DC sources:

If two DC sources with voltages E_1 and E_2 are present, the possible combinations are:

(i) Taking one level at a time: E_1, E_2, $-E_1$ and $-E_2$.

(ii) Taking two levels at a time: $(E_1 + E_2)$, $(E_1 - E_2)$, $(E_2 - E_1)$ and $-(E_1 + E_2)$.

(iii) Zero level: one.

Thus with two DC sources, there are nine possible combinations that can be obtained in the output waveform, resulting in a nine-level inverter. Such a structure is shown in Fig. 2b.

(c) With three DC sources:

If three DC sources with voltages E_1, E_2 and E_3 are present, the possible combinations are:

(i) Taking one level at a time: E_1, E_2, E_3, $-E_1$, $-E_2$, $-E_3$.

(ii) Taking two levels at a time: $(E_1 + E_2)$, $(E_1 - E_2)$, $(E_2 - E_1)$, $-(E_1 - E_2)$, $(E_2 + E_3)$, $(E_2 - E_3)$, $(E_3 - E_2)$, $-(E_2 + E_3)$, $(E_1 + E_3)$, $(E_1 - E_3)$, $(E_3 - E_1)$ and $-(E_1 + E_3)$.

(iii) Taking three levels at a time: $(E_1 + E_2 + E_3)$, $(E_1 + E_2 - E_3)$, $(E_1 - E_2 + E_3)$, $(E_1 - E_2 - E_3)$,

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($-E_1 + E_2 + E_3$), ($-E_1 + E_2 - E_3$), ($-E_1 - E_2 + E_3$) and $-(E_1 + E_2 + E_3)$.

(iv) Zero level: one.

Therefore, with three DC sources, there are 27 additive and subtractive combinations possible which result in a 27 level inverter.

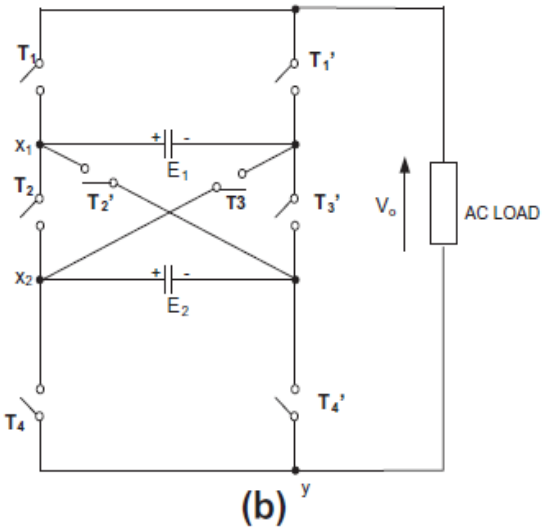

Fig.2b Inverter structure with two input DC sources

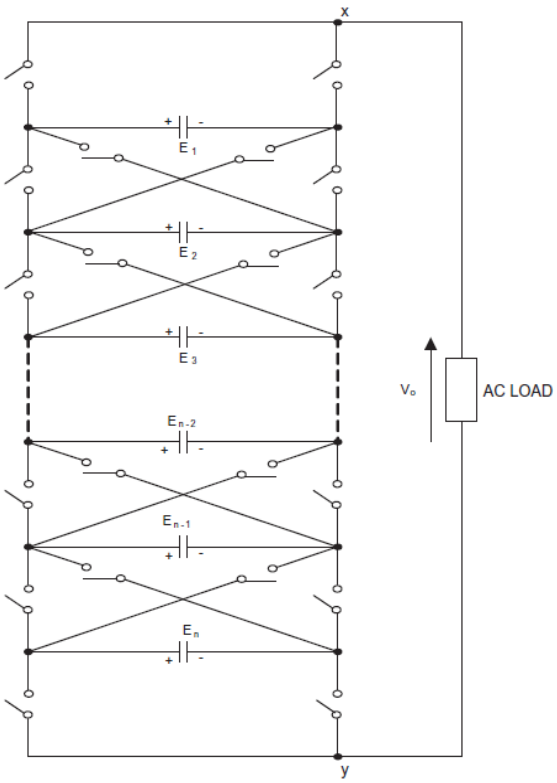

Fig.3 Generalized structure of proposed topology

The generalized expression for the number of levels can be obtained as:

Maximum number of levels = $(\sum_{m=1}^{n} \frac{n!}{(n-m)!} 2^m) + 1$ (1)

The term 'Maximum' is used in above expression because redundancy in the voltage levels may decrease the actual number of levels in the output. The generalized structure of the proposed topology is shown in Fig. 3. The arrangement of switches and DC sources are in such a manner that it is possible to obtain all possible combinations in the output. Moreover, if 'n' number of DC sources are present, then '4n' power switches are required to synthesize all possible combinations.

Therefore,

Total number of power switches required = 4n (2)

For example, Fig. 2b shows the proposed structure with two DC sources (obtained through independent sources or through DC link capacitors) capable of producing a nine level output. The power switches are paired as Tk and T'k, where k = {1, 2, 3, 4}. It is important to mention that switches Tk and T'k cannot be ON simultaneously, otherwise a dead short circuit appears across the source. In this sense they are designated to be 'complimentary'. However, this does not mean that the switching pulses to a complimentary pair are also complimentary, because to obtain any level only three switches need to be ON. For example, with switches T1, T3 and T4 ON, an output voltage level of E1 is obtained while with switches T1, T4 and T'2 ON a voltage level of -E2 is obtained. The detailed working is explained in the next section.

Table I summarizes the comparison between the classical multilevel topologies, conventional topology and the proposed topology in terms of component requirements for a nine-level output. It is seen that the device count is reduced significantly. While all the classical topologies require sixteen power switches each to deliver nine levels for a single-phase inverter, the conventional topology requires ten power switches whereas the proposed structure does so with eight switches. Of these eight switches, six are unidirectional and two are fully-directional. In addition, the proposed topology does not require clamping diodes or clamping capacitors.

IV. PRINCIPLE OF OPERATION

A. DC source arrangement

Following conditions for the DC voltage sources are assumed to maximize the number of levels in the output voltage:

(i) 'unary' arrangement will result if all the DC sources are equal, i.e.

$$E_1 = E_2 = E_3 = \ldots = E_n \quad (3)$$

(ii) 'binary' arrangement will result if the DC sources make a geometric progression with a factor of '1/2' i.e.

$$\frac{E1}{E2} = \frac{E2}{E3} = \ldots\ldots\ldots\ldots = \frac{En-1}{En} = 2 \quad (4)$$

(iii) 'trinary' arrangement will result if the DC sources make a geometric progression with a factor of '1/3' i.e.

$$\frac{E1}{E2} = \frac{E2}{E3} = \ldots\ldots\ldots\ldots = \frac{En-1}{En} = 3 \quad (5)$$

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TABLE I : Comparison of classical topologies, conventional topology and the proposed topology for nine level output.

Voltage Levels	Components	Classical topologies			Conventional topology	Proposed topology
		Diode clamped	Flying capacitors	Cascaded H-bridge		
9	DC Link capacitors	8	8	4	4	2
	Clamping diodes	56	-	-	-	0
	Clamping capacitors	-	28	-	-	0
	Gate drivers	16	16	16	10	8
	Power switches	16	16	16	10	Six unidirectional and two fully directional 8

For above three arrangements, the number of actual levels in the output waveform can be obtained using Eq. (1) and the results are summarized in Table II For two or more than two DC sources (i.e. for n > 1), trinary arrangement results in most number of levels as compared to other two arrangements.

TABLE II: DC source arrangements and corresponding number of levels

Sr. No.	Arrangement of DC sources	Number of levels in the output waveform
1	Unary (Em-1 = Em)	2n+1
2	Binary (Em-1 = 2 Em)	2(n+1) - 1
3	Trinary (Em-1 = 3 Em)	3n

B. Description of working states

The proposed topology with two input DC sources for nine-level output is shown in Fig.2b. The two sources are such that $E_2 < E_1$ and their arrangement (unary, binary or trinary) will decide the actual number of levels in the output. For example, by employing two sources E_1 and E_2 having equal values ($E_1 = E_2 = E_O$), five output levels (viz. $\pm E_O$, $\pm 2E_O$ and 0) can be obtained (i.e. a five-level waveform in steps of E_O). By employing a binary source configuration (with $E_1 = 2E_O$ and $E_2 = E_O$), seven output levels (viz. $\pm E_O$, $\pm 2E_O$, $\pm 3E_O$ and 0) can be synthesized (i.e. a seven-level waveform in steps of E_O). Similarly, a trinary source configuration (with $E_1 = 3E_O$ and $E_2 = E_O$) would synthesize voltage levels ($\pm E_O$, $\pm 2E_O$, $\pm 3E_O$, $\pm 4E_O$ and 0) i.e. a nine-level waveform in steps of E_O.

The topology has eight switches and to obtain any desired voltage level, three switches need to be ON.

There are four pairs of complimentary switches. Thus, three switches (to remain ON) can be chosen from four possibilities in ${}^4C_3$ (= 4) ways and each switch has two possibilities (either ON or OFF). Therefore, total number of states possible for the topology is $2^4 = 16$. In this single-phase configuration, the AC load is fed by nine levels ($E_1 + E_2$), (E_1), ($E_1 - E_2$), (E_2), (0), ($-E_2$), ($E_2 - E_1$), ($-E_1$) and $-(E_1 + E_2)$. It is also important to mention that any unbalance in input DC source magnitudes would not result in a multilevel waveform with equal voltage steps. All the possible states, voltage levels and switch positions are summarized in Table III, where redundant states are designated as (1, 1'), (2, 2'),(5, 5', 5", 5'"), (6, 6') and (7, 7'). Redundancy can be used for optimal switching of power semiconductor switches.

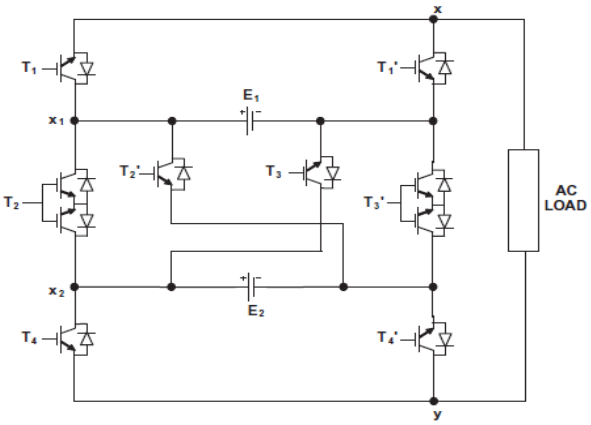

Fig. 3 Proposed configuration for single-phase nine-level Inverter

C. Power switch configurations

The proposed inverter can be realized with self commutating power switches like MOSFET's and IGBT's. It is also important to note that the switches at positions T_2 and T'_3 are necessarily required to be 'fully directional switches' otherwise their undesirable switching will take place.

Therefore, at both positions T_2 and T'_3, fully directional switches having the capability of blocking voltages in both directions are to be used. A common emitter combination is having low ON state drop but requires only one gate driver circuit. This switch configuration has been chosen for switches T_2 and T'_3 of the proposed multilevel structure with two DC sources as shown in Fig. 3.

D. Modulation Scheme

Multicarrier PWM and space vector modulation techniques have been employed for multilevel inverter modulation control [19–21]. These methods use high switching frequency, thereby causing extra switching losses. At the same time methods like active harmonic elimination [22], selective harmonic elimination (SHE) [22–24] and fundamental frequency method [22] are considered as low switching frequency methods.

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Sr. No.	States	Output level	Switching states (1 = ON, 0 = OFF)							
			T_1	T_2	T_3	T_4	T'_1	T'_2	T'_3	T'_4
1	1	E_1	1	0	0	0	0	0	1	1
2	1’	E_1	1	0	1	1	0	0	0	0
3	2	E_2	0	0	1	0	1	0	0	1
4	2’	E_2	1	1	0	0	0	0	0	1
5	3	E_1-E_2	1	0	0	1	0	0	1	0
6	4	E_1+E_2	1	0	1	0	0	0	0	1
7	5	0	0	0	0	0	1	0	1	1
8	5’	0	1	1	0	1	0	0	0	0
9	5”	0	0	0	1	1	1	0	0	0
10	5”’	0	1	0	0	0	0	1	0	1
11	6	-E_1	0	1	0	1	1	0	0	0
12	6’	-E_1	0	0	0	0	1	1	0	1
13	7	-E_2	0	0	0	1	1	0	1	0
14	7’	-E_2	1	0	0	1	0	1	0	0
15	8	E_2-E_1	0	1	0	0	1	0	0	1
16	9	-E_1-E_2	0	0	0	1	1	1	0	0

TABLE III: Various states for nine-level output

Though all the aforesaid methods can be used for the control of proposed structure, the control is demonstrated through low switching frequency multicarrier scheme [25, 26].

The carrier based PWM technique fulfils switching states by comparing a modulating signal V_A and a carrier waveform V_C .The modulating signal V_A is a sinusoidal at frequency F_C and amplitude V_A and the triangular signal V_C is at frequency F_C and amplitude V_C. In this topology phase opposition disposition-SPWM is adopted for its simplicity and all the carriers are in phase with each other as shown in Fig.4. The pulses so obtained are used for switching of device corresponding to the respective voltage levels [25].

However, in the proposed structure, various switches do not operate independent of each other. Therefore, the signals obtained from the comparison of the carriers and reference cannot be fed directly to the switches as done for two level inverters.

The overall modulation strategy is shown in Fig.5. In the proposed modulation scheme, for all the carrier waveforms above the time-axis, the results of comparison with the reference sine wave are ‘1’ or ‘0’. For all the carrier waves below the time-axis, the results of comparison with the reference sine wave are ‘0’ or ‘-1’. The signals so obtained are aggregated so as to synthesize an aggregated signal ‘As’.

The aggregated signal ‘As’ has same number of levels as desired in the output waveform. The switching signals are derived from this aggregated signal by comparing the signal with desired level using the lookup table and the output is fed to the switches. The look-up is shown in Table IV.

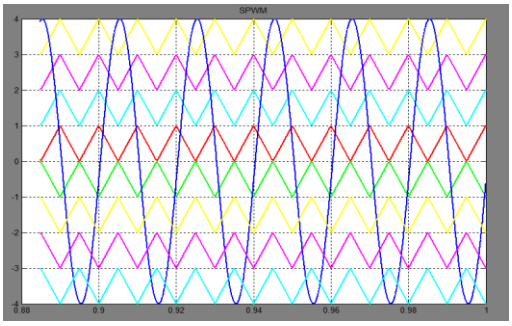

Fig.4 POD SPWM technique

V. SIMULATION RESULTS

Modulation techniques are used in multilevel inverter to synthesis a controlled output voltage. There are various modulation techniques, of which POD pulse width modulation is used here. Simulation of the proposed topology of multilevel inverter is performed using Matlab. Simulation results are shown in Fig.6 below. In this proposed topology, a modulating

TABLE IV: Look-up Table for proposed modulation scheme

A_s	Output Voltage	Switches states (1 = ON, 0 = OFF)							
		T_1	T_2	T_3	T_4	T'_1	T'_2	T'_3	T'_4
4	E1+E2	1	0	1	0	0	0	0	1
3	E1	1	0	0	0	0	0	1	1
2	E1-E2	1	0	0	1	0	0	1	0
1	E2	1	1	0	0	0	0	0	1
0	0	0	0	0	0	1	1	1	0
-1	-E2	0	0	0	1	1	0	1	0
-2	E2-E1	0	1	0	0	1	0	0	1
-3	-E1	0	1	0	1	1	0	0	0
-4	-E1-E2	0	0	0	1	1	1	0	0

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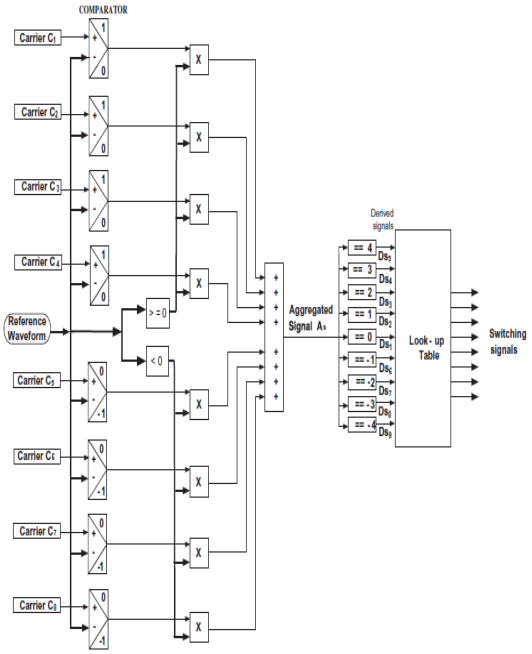

Fig.5 Proposed modulation scheme

The modulating signal is compared with eight carriers for a nine-level inverter and all the carriers are in phase and the pulses obtained through comparison are used for switching.

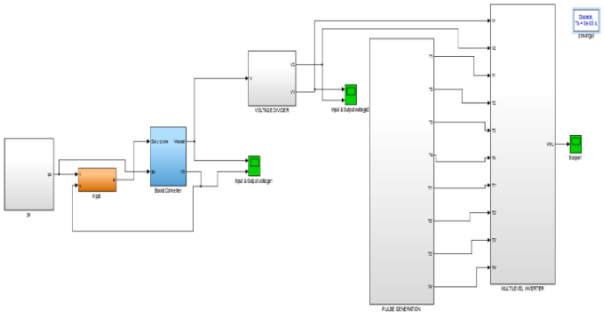

Fig.6 Simulation of proposed topology

DC supplies are powered through renewable energy source PV-MPPT system which is then boosted by the respective boost converter and the voltage obtained is divided in a suitable ratio in order to obtain the trinary arrangement. The inverter is operated in an open-loop mode and the switching frequency is 100Hz. Output voltage obtained is 324VP-P. The subsystem in Fig.7 shows the phase opposition disposition PWM generation. The resulting THD of the proposed system is shown in Fig.10.

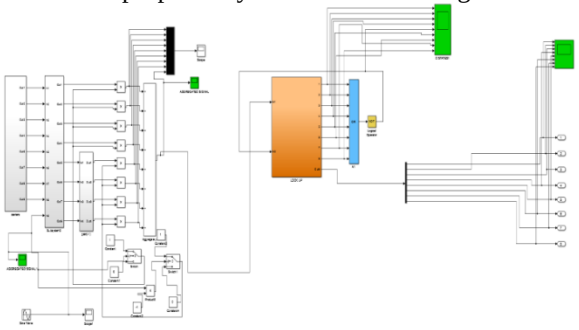

Fig.7 Subsystem of POD SPWM

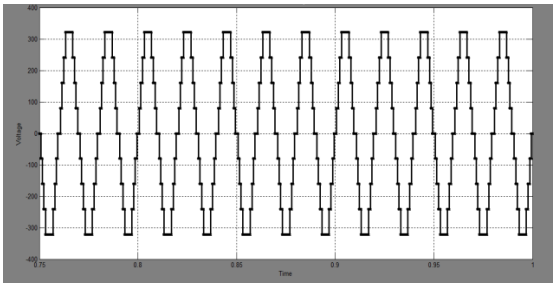

Fig.8 Output voltage of proposed nine level inverter

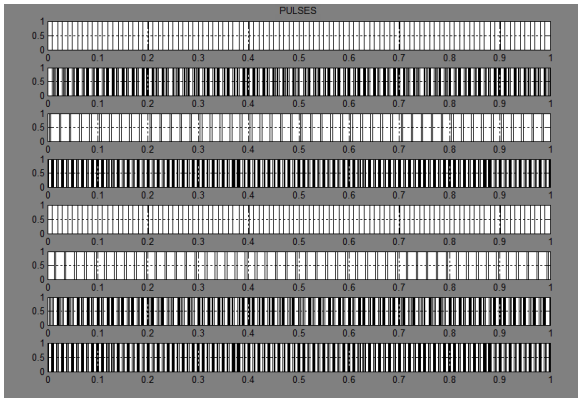

Fig.9 Gate pulses of proposed modulation scheme

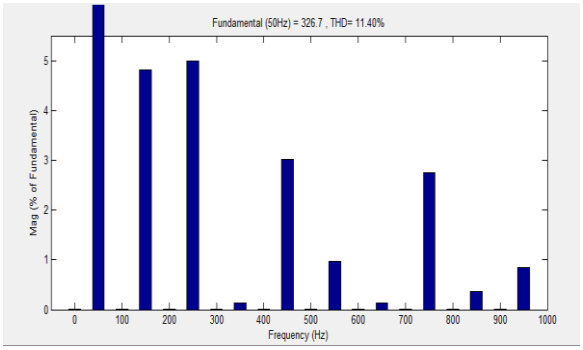

Fig.10 THD of nine-level inverter

VI. CONCLUSION

Multilevel inverters have been used in many industrial applications like HVDC, FACTS, EV, PV systems, UPS and industrial drive applications. A novel multilevel topology is proposed in this paper with a view to obtain all possible additive and subtractive combinations of the input DC levels in the output voltage waveform. It has less complex control method, less associated cost and lesser THD. The structure and principle of operation of the topology is detailed. Adaptation of Phase Opposition Disposition (POD) strategy sine pulse width modulation technique for the proposed structured is also explained. A comparison of presented topology with the classical and conventional topology shows that the device count is significantly reduced for a given number of levels in the output. The proposed concept is presented by simulations and verified experimentally for a single-phase nine-level inverter.

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